Journal of Electrical Engineering and Electronic Technology

Editorial

A SCITECHNOL JOURNAL

Advanced Techniques in VLSI Design for Achieving Ultra-Low-Power CMOS Circuits in Modern Electronics

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Citation: Priya M (2025) Advanced Techniques in VLSI Design for Achieving Ultra-Low-Power CMOS Circuits in Modern Electronics. J Electr Eng Electron Technol 14: 1012

Received: 01-Jul-2025, Manuscript No. JEEET-26-183671; **Editor assigned:** 3-Jul-2025, Pre-QC No. JEEET-26-183671 (PQ); **Reviewed:** 17-Jul-2025, QC No. JEEET-26-183671; **Revised:** 24-Jul-2025, Manuscript No. JEEET-26-183671 (R); **Published:** 31-Jul-2025, DOI: 10.4172/2325-9838.10001012

Introduction

Very Large Scale Integration (VLSI) technology has dramatically transformed the electronics landscape by enabling the integration of millions of transistors onto a single chip. As devices become smaller and more sophisticated, power consumption has emerged as a critical constraint, particularly for portable, battery-powered applications such as smartphones, wearable devices, and IoT systems. Complementary Metal-Oxide-Semiconductor (CMOS) technology remains the foundation of VLSI circuits due to its inherent low static power consumption and high noise immunity. However, as transistor scaling continues, issues like dynamic power dissipation, leakage currents, and switching losses increasingly affect performance and energy efficiency. Consequently, the design of low-power CMOS circuits has become a central focus in VLSI research, aiming to achieve high-performance operation while minimizing energy consumption [1,2].

Discussion

Power dissipation in CMOS circuits primarily arises from three sources: dynamic power, short-circuit power, and static leakage power. Dynamic power, caused by charging and discharging load capacitances during transistor switching, is the dominant factor in high-frequency VLSI circuits. Techniques such as clock gating, power gating, and reducing switching activity are widely used to minimize dynamic power. Clock gating selectively disables unused portions of a circuit, preventing unnecessary transitions and conserving energy, while power gating cuts off power to idle blocks entirely [3,4].

Leakage power, which becomes significant in deep-submicron technologies, results from subthreshold conduction, gate oxide leakage, and junction leakage. Low-power design strategies at the transistor level include multi-threshold CMOS (MTCMOS), transistor stacking, and body biasing to reduce leakage currents without severely impacting circuit speed. Optimizing transistor sizing and threshold voltages also helps balance energy efficiency, performance, and chip area [5].

At the architectural level, system-wide strategies such as dynamic voltage and frequency scaling (DVFS) and adaptive clocking further enhance energy efficiency. Memory-aware techniques and data-driven computation methods reduce unnecessary switching in data-intensive applications. Additionally, emerging device technologies like FinFETs and SOI (Silicon-On-Insulator) transistors provide superior leakage control and support aggressive low-power designs. Modern EDA (Electronic Design Automation) tools facilitate early-stage power analysis, enabling designers to optimize low-power CMOS circuits effectively during the design cycle.

Conclusion

Low-power CMOS circuit design is a cornerstone of modern VLSI technology, driven by the demand for energy-efficient, high-performance electronic systems. By combining transistor-level, circuit-level, and system-level strategies, designers can significantly reduce power consumption while maintaining reliability and performance. Advances in device technologies, architectural optimization, and power-aware design tools continue to expand the possibilities of low-power VLSI circuits. As portable electronics and embedded systems become increasingly ubiquitous, the development of energy-efficient CMOS designs will remain critical for sustainable and high-performance computing solutions.

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