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Development of High-Power Rectifier for Power Factor Correction Using Interleaved Boost Topology

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Abstract

In this paper, a 2KW rectifier with power factor correction is designed and developed. The converter is applied for server application, which adopts two phase interleaved boost converter (IBC). The circuit operates in continuous current conduction (CCM) mode and use a cascade control strategy. Cascade control has two loops; inner current loop uses average current control and outer voltage loop uses PI control strategy. In order to verify feasibility of proposed scheme, firstly; a 2KW IBC type PFC is simulated using PSIM software and then a prototype is developed which is converting 180-260V AC input voltage to 400V DC output voltage, is implemented using a Microchip IC dsPIC33FJ16GS504. The experimental results are satisfactory, which reveal that a power factor is 0.9992 (close to unity), THD less than 5% and more than 98% efficiency at 100 KHz switching frequency, 230Vrms input voltage and power output from 400W to 2KW.

Keywords: Two Faze interleaved boost converter; CCM; power factor correction; PI control; wide voltage input range; 16 bit micro-controller

Introduction

In the present time, greater part of the electronic gadgets use DC supply. Transformation of AC to DC is comprehensively used in various applications, for example, Switched Mode Power Supplies, battery chargers, power supplies to communication systems, washing machines, air-conditioners, servers, and so on. Because of presence of diodes, ordinary rectifiers followed by substantial size capacitors for energy storage, acts as a nonlinear load to power line and the power factor of such circuits is very low, even lower than 0.7. Ordinary rectifiers have irregular and non-sinusoidal line currents injecting large amount of harmonics in line and polluting the power supplies. These low order line current harmonics distorts the voltage at common coupling. In addition to voltage distortions, it also increases current ratings of line, due to large currents; heating of the equipment's, low efficiency, large size line filtering requirement are some of the drawbacks. Therefore to avoid all these consequences and to improve power quality as per the international standards an appropriate power factor corrector must be used [1].

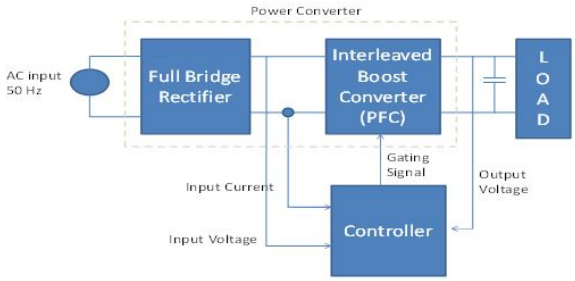
Numbers of active and passive circuits were utilized by numerous specialists to address this issue [3], [12]. The most straightforward approach is to use passive PFCs which improves power factor to somewhat acceptable level. Out of the solutions available in literature, passive PFCs are effective for low power applications most extreme up-to 200W. Disadvantages of passive PFCs are enormous in size, critical reliance of average output voltage on load change and are more expensive. To resolve this issue active PFCs were suggested by many researchers [4].

In this paper, two main converter topologies, boost and interleaved boost are investigated and analyzed for enhancing PF, THD and efficiency in single phase power supply. Both topologies are operated at switching frequency 100 kHz with 2 kW output power and 400V output DC voltage to provide THDi less than 5%, efficiency greater than 95% and PF close to unity [2].

The paper is structured in the following manner: The control strategy for both a boost and interleaved boost converter is presented in the second section. Afterward, in third section the design of the converter system with average current control is explained. The fourth section is dedicated to present the results of simulation using PSIM software. The fifth section shows the experimental results and explains micro-controller-based implementation of real-time model. Finally, conclusions are conferred in the last section.

The block diagram of interleaved PFC converter based on average current control is shown in Fig.1. Power converter uses a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage, followed by a interleaved boost converter which acts as an active PF corrector. For controlling the output voltage and correcting the input power factor, the dc output voltage, input ac current and input ac voltage are given as a feedback signals to the controller. Controller has its own reference levels and according to the error it manipulates the actuating signals and provides the gate signals to the active device MOSFETs to control the output voltage and input power factor.

Figure1: Block Diagram of 2KW PFC Interleaved Boost Converter and its control.

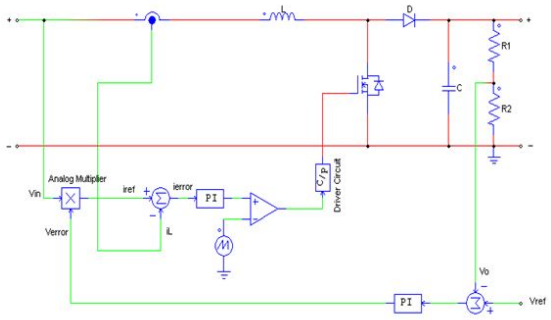


Proposed Interleaved Boost Topology and Control Strategy

PFC by Average Current Control using Boost Topology:

There are distinctive current mode control techniques like variable frequency Peak current control, Hysteresis control, and average current control. Out of which average current control demonstrates better outcomes. It is more desired than other control strategies because line current can be approximated by the average of current per switching cycle [7]. The fundamental circuit diagram of Boost converter is shown in Fig.2. For regulation of output voltage and simultaneously correction of power factor here cascade control is utilized. There are two loops in cascade control: inner loop and outer loop. Outer voltage loop maintains the output voltage to a set value and inner current loop does the job for power factor correction by continuously comparing input current IL with reference current Iref. By utilizing PI controller alongside PWM technique, gate signals are generated which controls on time i.e., duty cycle of the active switching device.

Figure 2: Average current control strategy for boost converter.



PFC by Average Current Control using Interleaved Boost Topology:

In conventional boost topology, volume of inductor is substantially large, and ripple current cancellation is not possible. These limitations can be overwhelmed by utilization of interleaved boost converter (IBC). IBC comprises of two boost converters connected in parallel, operating at 180° phase shift. The input current is the addition of two inductor currents. As the ripple currents streaming in two inductors are out of phase, they tend to cancel each other and so total harmonics in the input side is decreased. At 50% duty cycle, cancellation of ripple current is the most ideal.

Capacitor current in the output is the sum of two diode currents (ID1) and ID2) minus the load current (IL). Fs is the switching frequency, Ts is the time-period of one switching cycle and D is the Duty cycle. During the D*Ts period, switch S1 is ON and inductor current IL flows to energize the inductor. During the period (1-D*Ts) of the switching cycle, S1 is OFF but inductor current cannot change instantly. The inductor current starts decreasing. This change in current di/dt creates adequate voltage (L*di/dt) across the inductor with a polarity such as to drive current through diode D1 to charge the output capacitor [6].

A fundamental boost PFC converter converts a DC voltage to a larger DC level. The interleaved boost PFC increases the voltage level, however as it comprises of two boost converters in parallel so includes the advantage of two phases activated at 180 degrees out of stage [7]. Conduction losses in the switches and diodes can be decreased by partitioning the current into two power paths, which finally results in gain of overall efficiency compared to a boost converter. As effective ripple frequency at output is doubled, making ripple voltage reduction much easier, hence the power loss in overall circuit is reduced [10]. The circuit diagram of IBC converter is shown in Fig.3a. Vin the source input voltage, VL1 and VL2 are the voltages across L1 and L2 respectively. IL1, IL2 are the currents flowing through inductor L1 and L2 respectively. Ic and Io are currents flowing through output capacitor and load. Modes of operation of the interleaved boost topology are shown in Fig.3.

In mode1 appeared in Fig.3b, switches S1 and S2 are ON, diodes D1 and D2 are OFF, current through L1 and L2 increases depending on input voltage and stores the energy in L1 and L2. The sum of VL1 and VL2 during this time is Vin. A inductor current increments linearly with the slope of Vin/2L. During this time the current through S1 and S2 is same as IL1 and IL2 respectively. In mode 2, S2 turns OFF, D2 turns ON as the input voltage becomes higher than the output voltage to deliver part of its stored energy to the load and output capacitor as shown in Fig.3c. The current in L2 inclines down with a slant subject to the contrast between the input and output voltage. Mode 3 is similar to Mode 2 here S1 turns off and D1 turns on as shown in Fig.3d. The current in L1 inclines down with a slope dependent on the difference between the input and output voltage in Mode 4 as shown in Fig.3 (e), S1 and S2 are off, both L1 and L2 deliver their part of energy to the load and the output capacitor, as a result current in L1 and L2 ramps down. For controlling of interleaved boost converter using PI average current control technique the sensing of output voltage, input currents and the input voltage is necessary [15]. An opto-coupler and potential transformer are used to sense the input voltage [5], [10]. An input current is detected by using current transformer or Hall- effect sensor. Here two boost converters are connected in parallel to share the total load as shown in interleaved boost converter. Each converter will deliver only the portion of the power that it is programmed for by its reference current limit [15].

Figure 3: Circuit configuration of a Interleaved Boost PFC converter: a) With operational switch: - b) Mode 1 S1andS2 ON, c) Mode 2 S1ON and S2 OFF, d) Mode 3 S1 OFF and S2 ON , e) Mode 4 S1 and S2 OFF.

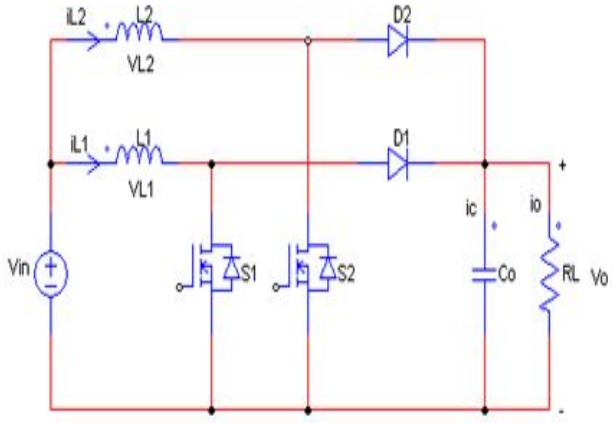


Figure 3.a

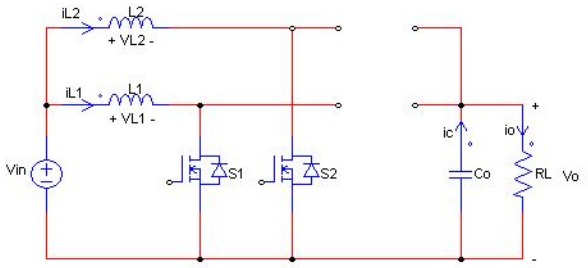


Figure 3.b Mode 1

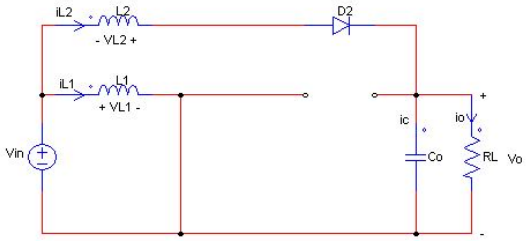


Figure 3.c Mode 2

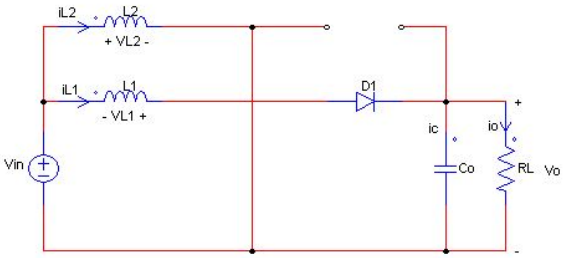


Figure 3.d Mode 3

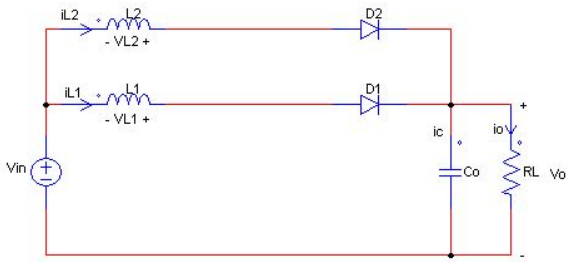


Figure 3.e Mode 4

The inductor currents iL1 and iL2 with the output capacitor voltage Vo are assumed as state variables. The converter comprises of four modes of operation.

Mode1 : Switches S1 and S2 are ON, diode D1 and D2 are OFF. At this stage, the state differential equations of the circuit are given by:

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2}$$

$$\frac{dV_o}{dt} = \frac{-V_o}{RC}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} V_{in} \quad (1)$$

Mode 2: Switches S1 diode D2 are ON, and S2 and D1 are OFF.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2} - \frac{V_o}{L_2}$$

$$\frac{dV_o}{dt} = \frac{i_{L2}}{C} - \frac{V_R}{RC}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} V_{in} \quad (2)$$

Mode 3: Switch S2 and diode D1 are ON, and Switch S1 and diode D2 are OFF.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{V_o}{L_1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2}$$

$$\frac{dV_o}{dt} = \frac{i_{L1}}{C} - \frac{V_R}{RC}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} V_{in} \quad (3)$$

Mode 4: Switches S1 and S2 are OFF, diode D1and D2 are ON.

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{V_o}{L_1}$$

$$\frac{di_{L2}}{dt} = \frac{V_{in}}{L_2} - \frac{V_o}{L_2}$$

$$\frac{dV_o}{dt} = \frac{i_{L1}}{C} + \frac{i_{L2}}{C} - \frac{V_R}{RC}$$

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} V_{in} \quad (4)$$

Design Parameters For Proposed Topology

The key circuit parameters and specifications are listed as bellow:

Vin (t) = 180V～260V,

Vo = 400VDC ± 1%

Po =2000W, Fs= 100kHz

Lin= 520µH for Boost, L1= 520µH, L2=520µH for IBC,

Co= 1410µF

where Vin(t) is the AC RMS input voltage, Vo is the regulated output dc voltage, Po is the output power, Fs is the switching frequency, Lin is the boost inductance, Co is the output capacitance.

Design for Boost Inductor

The design of boost inductor is a critical part. The inductor determines amount of ripple current in the input current. The inductor is to be designed at the minimum input voltage of circuit [7]. At full load current, and when the input voltage is minimum; the maximum current flows through inductor, the corresponding maximum duty cycle is given by:

$$d = [V_o - \sqrt{2} * V_{in\,(min\,pk)}] / V_o \quad \ldots (5)$$

And, boost inductor is calculated by:

$$L_1, L_2 = [V_{in\,(min\,pk)} * d * T_s]/d_I \quad \ldots (6)$$

Where, Vin (min pk) is the minimum peak input voltage, Vo is output voltage, d is maximum duty ratio,

Ts are the time period of one switching cycle, and dI is allowed ripple current in percentage [9].

Design for Output Capacitor

The output capacitor for PFC pre-regulator is selected as per the requirement of hold-up time. Hold up time is the function of energy storage capacity of the capacitor, load power and the minimum and maximum limits of the output voltage.

The value of Comin is given by:

$$C_o = [2 * P_{out} * t_h] / [(Vo_{(max)})^2 - (Vo_{(min)})^2] \quad \ldots (7)$$

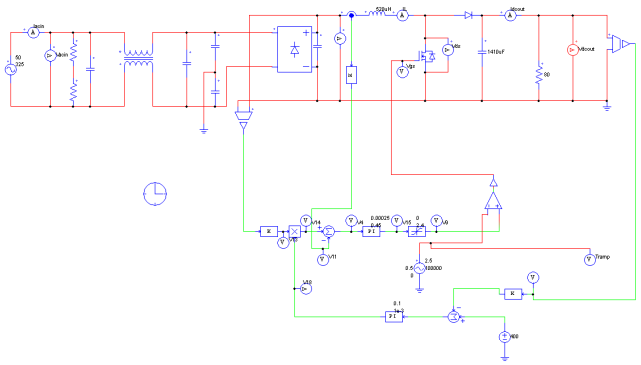
Where, Pout is the maximum output power, th is the hold- up time , Vo(max) is the maximum output voltage and Vo(min) is the minimum output voltage.

Controller Design

Control Strategy of Average Current Mode for Conventional BOOST topology:

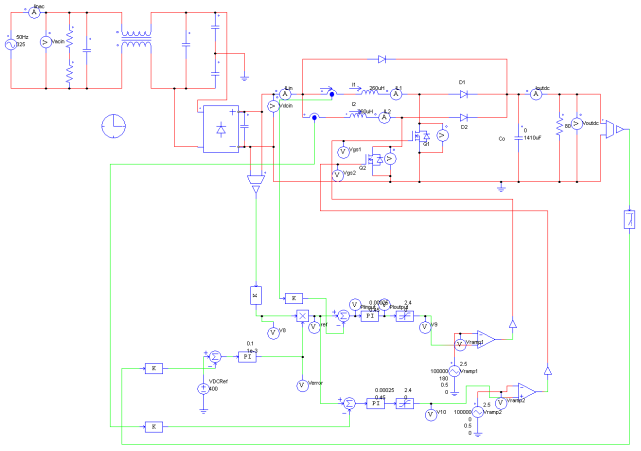
Control technique with Average Current Mode for conventional boost converter is shown in Fig. 4. The current passing through inductor L (iL) is compared with the reference current (iref), and is processed using current error amplifier. Then, the average error current, is amplified, compared with the triangular wave, and which provides the PWM drive signal for the switching transistor. When the inductor current iL increases, the error current I error decreases, the output duty cycle for PWM comparator decreases, results in reduced inductor current iL. In contrast, the inductor current iL increases. When the desired output voltage Vo increases, the output of comparator decreases, so error current I error decreases, the output duty cycle for PWM comparator decreases, results in less inductor current iL and output voltage Vo. In contrast, the output voltage Vo increases.

Figure 4: Simulation Circuit of Average current control strategy for Boost converter Control Strategy of Average Current Mode for Interleaved BOOST topology:



In high power applications, to overcome the limitations of the boost converter, interleaved boost converter is a better choice. The IBC takes advantage of ripple reduction and input power sharing between the different converters connected in parallel. Due to the distribution of input power and low circulating harmonic currents, the magnetic volume is greatly reduced [13]. In addition, as ripple content in the output is less which avoids additional output filter requirement [12]. Fig.5 shows the interleaved boost converter with two boost phases triggered with a phase shift of 180º. A few disadvantages of this topology are the number of components, implementation cost is moderate and little more control complexity, as presented by [3], [4].

Figure 5: Simulation Circuit of Average current control strategy for Interleaved Boost Converter.



Simulation results

A 2000W **model is simulated using PSIM software to assess Boost converter and Interleaved Boost converter with PI average current control strategy. The Input** AC RMS voltage is 230 V and the output D C **voltage is** 400V. **The AC input voltage-current waveforms and DC output voltage-current waveforms of boost converter and interleaved boost converter are shown in Fig. 6a and Fig. 6b, respectively. And the Fast Fourier Transform (FFT) of ripple current in boost converter and interleaved boost converter are shown in Fig. 7a and Fig. 7b, respectively. The rectified AC input is boosted using Boost and Interleaved boost converter. For closed loop operation in real time implementation input voltage, inductor current and output voltage will be sensed using current transformer and potential transformer. The converters are operated at 100 kHz switching frequency,** 2000W **output power with the reference voltage of** 400V.

Table I: PSIM Simulation Results of Boost Converter Pout= 2000Watts L = 520uH, Co = 1410uF.

Sr. No	Vin AC Vrms	Iin AC (A)	Pin (W)	RL (Ω)	Vout DC (V)	Iout DC (A)	Pout (W)	P. F.	THD %	Effi %
1	230	12.56	2021	80	400.39	5.00	1998	0.9949	8.44	98.86
2	230	9.97	1616	100	400.44	4.00	1597	0.9935	8.80	98.22
3	230	7.42	1228	133	400.37	3.00	1201	0.9912	9.17	97.80
4	230	4.92	822	200	400.00	2.00	798	0.9862	10.30	97.10
5	230	3.3	561	300	399.30	1.33	530	0.9791	12.30	94.46
6	230	2.47	434	400	397.32	0.99	393	0.9735	15.20	90.58

Table II: PSIM Simulation Results of IBC Interleaved Boost Converter Pout= 2000Watts L1 =L2= 520µH, Co = 1410µF.

Sr. No	Vin AC Vrms	Iin AC (A)	Pin (W)	RL (Ω)	Vout DC (V)	Iout DC (A)	Pout (W)	P. F.	THD %	Effi %
1	230	12.77	2032	80	399.41	4.99	1996	0.9993	3.46	99.46
2	230	10.18	1630	100	399.2	3.99	1593	0.9984	4.62	98.72
3	230	7.7	1233	133	398.21	2.99	1192	0.9965	6.12	96.63
4	230	5.25	845	200	393.68	1.97	775	0.9917	9.97	91.75
5	230	3.52	568	300	398.66	1.32	530	0.9815	11.9	93.05
6	230	2.9	427	400	400	1	399	0.9812	16.3	93.5

Figure 6a: Input-Output Waveforms of Boost Converter.

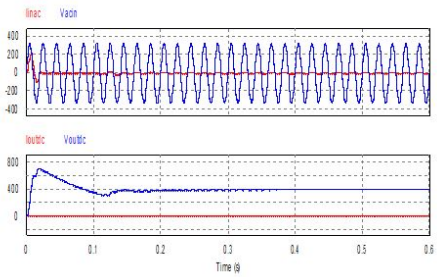


Figure 6b: Input-Output Waveforms of IBC Converter.

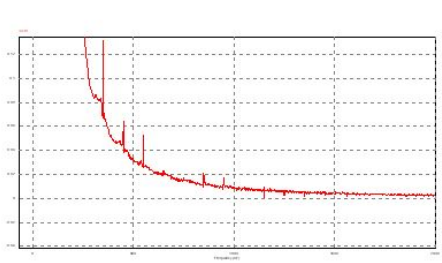


Figure 7a: Fast Fourier Transform of ripple current in Boost Converter.

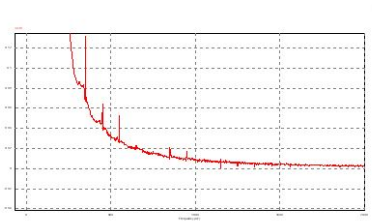


Figure 7b: Fast Fourier Transform of ripple current in Interleaved Boost Converter.

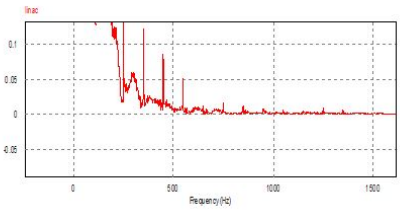


Figure 8a: THD versus Output Power for Boost and IBC.

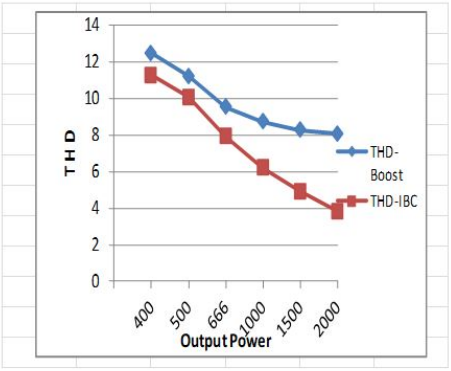


Figure 8b: PF versus Output Power for Boost and IBC.

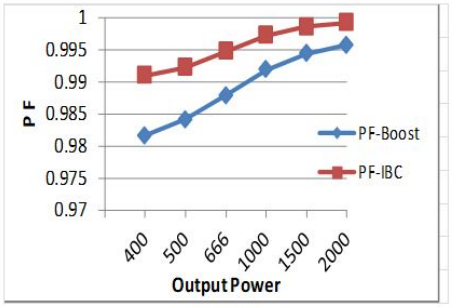


Figure 8c: Efficiency versus Output Power for Boost and IBC.

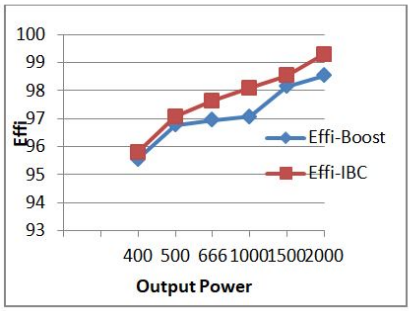


Table III: Comparative Performance of PSIM Simulated Results.

Topology	P.F.	T.H.D. %	Efficiency %
Boost	0.9949	8.44	98.86
IBC	0.9993	3.46	99.46

The comparative Simulation performance of conventional Boost, and Interleaved Boost Converters (IBC) based PFC is shown in Table III for 230Vrms AC input at 100 kHz switching frequency, 2KW output power and 400V dc output voltage. Fig.8a, Fig.8b and Fig.8c shows THD, PF and overall efficiency comparison of boost and IBC topology, respectively. Simulation results reveal that, the overall efficiency of the IBC type converter has improved i.e., 99.46% compared to boost type converter. The THD has been reduced to

3.46% which is as per the IEC61000-3-2 Standards and there is an improvement in power factor 0.9993.

As exhibited through this paper, interleaving boost type rectifiers provide high frequency input current ripple cancellation. Because of decreasing amplitudes of the input current ripple, there is a decrease in filter size. A comparison of boost and interleaved boost type PFC revealed that the interleaving is a extremely successful technique for lessening input line current harmonics.

Experimental results

An experimental prototype of high-power rectifier based on average current control with IBC topology, which is controlled by dsPIC33fj16gs504, is developed to confirm the operational working of the proposed converter. Fig.9 shows the experimental prototype for proposed 2KW Interleaved Boost PFC converter. Components and devices used are recorded in Table IV.

Table IV: Devices and Components used for Experimental Model.

Parameter	Manufacturer	Value
CoolMOS Power MOSFETs	Infineon Technologies	SPI20N60C3
Boost Diodes	IXYS	DSEI60-12A
Full-Bridge Rectifier	International Rectifier	GBU25J
Boost Inductor	Neha Tech Services	550µH
Output Capacitor	ALCON Electronics	2200µF
Load Resistor	-	80-400Ω
Current Sensor	Neha Tech Services	Current Transformer CT
Voltage Sensor	-	Potential Divider

Prototype

Figure 9 demonstrates the picture of hardware model: the power circuit, control card and auxiliary power supply. The power circuit contains the high power converter and the regulated auxiliary power supplies for the control circuit. The control PCB contains the signal conditioning circuits and the micro-controller. The power stage is the well-known circuit and; hence, we mention only the characteristics of control circuit.

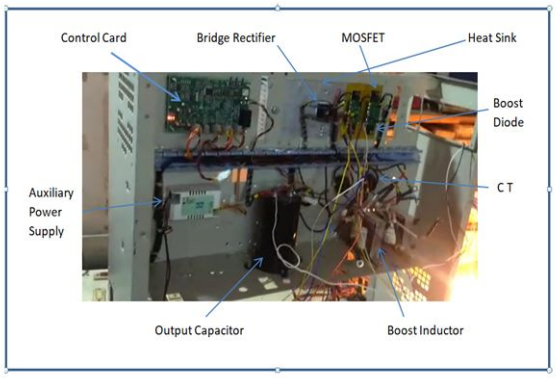
A 16-bit micro-controller dsPIC33FJ16GS504 from Microchip technologies is used for controlling the converter. The micro-controller operates with clock frequency of 40 MHz. We have used five ADCs simultaneously operating at same sampling rate.

The input current sensed by Shunt resistance is amplified by differential amplifier and fed to the analog channel of the ADC (0 - 3.3v).

The sensed output voltage is conditioned by a potential divider and to minimize the ripple current in the output it is filtered by a low-pass filter with cut off frequency of 88Hz.

A +12V auxiliary power supply is necessary to feed the gate drive circuit. To feed the micro-controller an auxiliary source of 5V has been used. The gating signals for MOSFETs are generated with a driver circuit IC MCP1403 of Microchip Technologies.

Figure 9: Pictures of the Experimental Model: a) Power Circuit, b) Control Card, c) Auxiliary Power Supply.



Algorithm

The control algorithm functions with internal timer interruption which is defined to be of a sample time 50uS. In inner current control loop for the purpose of data acquisition and AtoD conversion it needs 27uS. The difference equation of voltage controller is segmented to distribute the computational charge cycle-by-cycle. Hence, the total sample time does not surge substantially, and the sample time required for the outer control loop can be defined easily. We have defined the sample time of 500uS for the outer voltage control loop.

Table VI: Results of Hardware implemented IBC Interleaved Boost type high power Converter L1 =L2= 550µH, Co = 2200µF.

Sr. No	Vin AC Vrms	Iin AC (A)	Pin (W)	RL (Ω)	Vout DC (V)	Iout DC (A)	Pout (W)	P.F.	THD %	Effi %
1	230	13.50	2030	80	399.50	4.98	1990	0.9992	4.11	98.00
2	230	11.00	1630	100	399.20	3.94	1575	0.9980	4.82	96.62
3	230	8.50	1152	150	398.10	2.76	1100	0.9930	6.38	95.48
4	230	6.50	745	200	393.20	1.75	700	0.9810	9.00	93.95
5	230	4.00	525	300	398.50	1.23	490	0.9800	12.15	93.33
6	230	3.00	400	400	400	0.923	368	0.9780	17.3	92.00

Figure10a: THD versus Output Power for Prototype IBC.

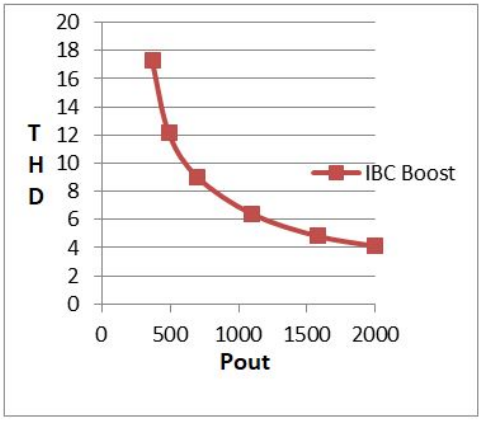


Figure10b: PF versus Output Power for Prototype IBC.

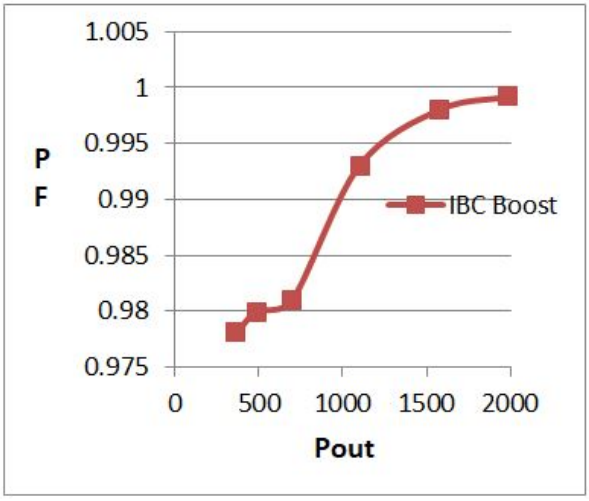
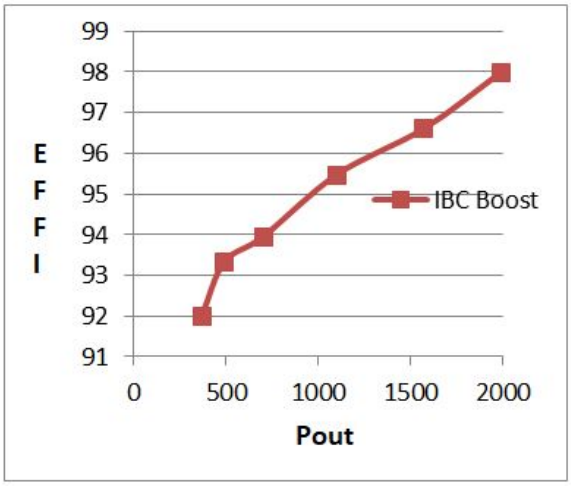


Figure 10c: Efficiency versus Output Power for Prototype IBC.



Results and Discussion

Table VII: Comparative Analysis of PF, THD and Efficiency of Proposed Converter.

Topology	P.F.	T.H.D. %	Efficiency %
Boost Simulation	0.9949	8.44	98.86
IBC Simulation	0.9993	3.46	99.46
IBC Prototype	0.9992	4.11	98.00

PSIM Simulation results for IBC type PFC converter are shown in Fig.9a, Fig.9b and Fig.9c. Results obtained from experimental model are presented in Fig.10a, Fig.10b and Fig.10c, respectively.

The proposed 2KW IBCPFC Converter which is having two-phase interleaved boost PFC have the subsequent features:

As in IBC two boost topologies are switching at 180 degree, i. e. out of phase, their inductor currents are also staggered and cancel with each other; so effective ripple in input current is reduced. So THD is reduced. As switches are operated at high frequency, and ripple current is twice for each phase, which reduces required size of EMI filter. As high-frequency ripple current in the output capacitor is reduced, so required value of output capacitor declines. Finally, input line current wave tracks better the input voltage wave, so the power factor is very high.

Conclusion

In this work, a front-end 2KW interleaved boost type PFC converter for power factor correction is proposed using PI controller in CCM mode. The feasibility and reliability of the proposed converter is first verified by simulation in PSIM software and then confirmed by a hardware prototype model. As per simulation results, the conventional boost converter has overall efficiency of 98.86% and THDi = 8.44%, PF 0.9949 and the interleaved boost converter has efficiency of 99.46 % and THDi = 3.46%, PF = 0.9993. Simulation results are confirmed by the hardware prototype implementation of the developed converter. According to results of implemented model, the overall efficiency is 98.00%, THDi is = 4.11% and PF is = 0.9992. At last, the THD measured on prototype model is in great agreement with the results obtained by simulation and is fit in with IEEE and IEC standards.

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