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Fabrication and Experimental Verification Energy Reversible SoI-NEM Switch for Adiabatic Computation and Bio-Medical Applications

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Abstract

In this work, we present the theoretical analysis and experimental verification of energy reversible Nano Electromechanical Switch (NEMS) for adiabatic computations and bio-medical applications. At its core, adiabatic circuits reduce power consumption significantly during logic operations using a four-phase power clock along with clever circuit arrangements which avoid the buildup of charges across a single transistor. The NEM switches can prove to be the ideal building blocks for these electronics chips as they present no leakage-current and therefore consumes very low static power. In particular, the energy reversible NEM switches can further reduce the power consumption in adiabatic circuits, since these switches conserve and reuse the mechanical bending energy stored in them in the first cycle, and for subsequent switching cycles. In this work, we have reported theoretical analysis and experimental proof of the benefits of using NEM switches (three-terminal and energy reversible, both) in place of traditional Complementary Metal Oxide Semiconductor (CMOS) transistor switches in adiabatic circuits, in terms of the energy dissipation per unit cycle of power clock for various power clock frequencies. Here, we have observed that the experimentally observed reduction in pull-in voltage (13%) for subsequent cycles of switching for energy reversible NEM switches, indicating a reduction in switching energy. It is found that the NEM switches promise to offer lower energy consumption for low-frequency operations (<100 kHz) and therefore it is recommended that it is best suited for biomedical and low-power applications.

Keywords: Adiabatic Computing; Bio-Medical; NEMS; Static Power

Introduction

Adiabatic computation and at its core adiabatic circuits have gained momentum inrecent years for low power logic applications [1-5]. The term "adiabatic" has been historically associated with a thermodynamic system with gradually changing parameters such that the energy in the system is conserved [6-8]. Similarly, adiabatic logic circuit proposes to conserve the charge in a circuit by exchanging the charge from the load to the supply in a complete switching cycle [9,10]. An adiabatic circuit design requires the use of power clocks to simulate a slow change in the system and complex circuitry to ascertain that no transistor observes an abrupt change in potential across its terminals. An exchange of charges, by definition, requires the flow of current [11]. In the case of adiabatic circuits, the current flows from the supply voltage to the load capacitance during the charging cycle and back during the discharge cycle. Consider a simple circuit with a voltage source (Vdd) connected to a load capacitance (CL) through a series resistance (Rs). The inherent resistances associated with the metal wires and power supply are included in the lumped resistance (Rs). For charge exchange, the current must flow through this resistance. As in the case of thermodynamic systems, this process is carried out slowly, so that, at any given point of time, a smaller potential difference exists across the resistance, thus restricting the current levels. In the ideal case, this process requires infinite time so that the current through the series resistance tends to zero and the power consumed also tends to zero. Let the total time taken for the charge transfer is T. The steady current required for this charge transfer is given by:

$$I = \frac{C_L V_{dd}}{T} \quad (1)$$

The total energy dissipated during a full charge exchange is given by:

$$E_{ad\$a} = 2 \times I^2 R_s T \quad (2)$$

$$E_{ad\$a} = \frac{2C^2V^2\ R}{T} \quad (3)$$

Here, the energy dissipation can be reduced by reducing the Vdd, CL, and Rs. Also, as in thermodynamics, a slower process takes lower energy, and an infinitely slow process is reversible (zero-energy consumption). Now, this is the energy required to exchange charges adiabatically, regardless of the implementation of the logic circuit. Hence, this analysis holds true for all Complementary Metal Oxide Semiconductor (CMOS) circuits [12,13]. Adiabatic CMOS circuits have been realized in several configurations [14-17]. These circuits make sure that there is no sudden switch-on or a surge of charging current that results in high power dissipation. The power is supplied through a four-phase power clock, Figure 1.

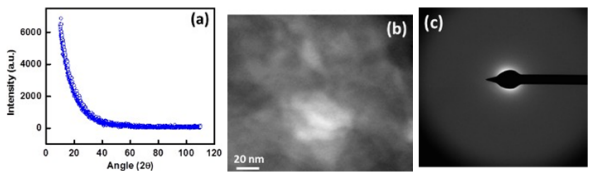

Figure 1: The four phases of the power clock that are used to regulate adiabatic circuits. (a) X-ray diffraction plot showing pristine amorphous structure of WNx. (b) HRTEM image showing no

existence of crystalline clusters or grain. (c) TEM diffraction pattern shows no existence of any type of crystal clusters.

In the case of a regular CMOS circuit, there is always an inherent leakage current is present at lower technology nodes. Since this current is present across the entire supply voltage (i.e., from the power supply to the ground terminal), it causes a significant power loss. In the case of adiabatic circuits, this current is only significant in one of the four power clock phases, Figure 2.

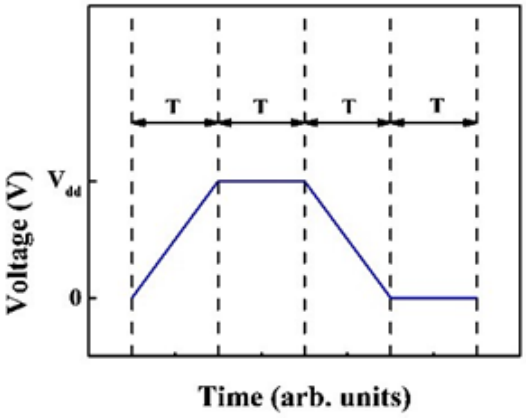

Figure 2: The four phases of the power clock are used to regulate adiabatic circuits with ramp-up and ramp-down sym-metry.

The total energy consumption can be obtained by integrating the leakage current over the four power clock phases. Assuming symmetry across the two clock phases (ramp- up and ramp-down), the leakage energy is given by:

$$E_{leak} = 2 \times \int_0^T \frac{tV_{dd}}{T} I_{off} \left(1 - e^{-\frac{tV_{dd}}{V_t T}}\right) dt \; + \; I_{off} V_{dd} T \qquad (4)$$

Where, Ioff is the off-state leakage current for a MOSFET, Vdd is the supply potential, Vt is the thermal potential.

Here, the first term denotes the leakage current during rise-time and fall-time of the power clock. The second term represents the leakage during peak phase of the power clock. So, from Eq (4),

$$E_{leak} = 2I_{off} V_{dd} T + \frac{2I_{off} V_t^2 T}{V_{dd}} \left(1 - \left(1 + \left(\frac{V_{dd}}{V_t}\right)\right) e^{-\frac{V_{dd}}{V_t}}\right) \qquad (5)$$

Considering, $e^{-\frac{V_{dd}}{V_t}} \sim 0$, we have:

$$E_{leak} = 2I_{off} V_{dd} T \left(1 + \frac{V_t^2}{V_{dd}^2}\right) \qquad (6)$$

This leakage energy is directly proportional to time. Thus, contrary to the adiabatic charge transfer energy, an increase in charge transfer time (or power clock time-period) will result in an increase in energy dissipation in a CMOS circuit. This result is intuitive since a larger time period will provide more time for leakage currents to dissipate power. The total energy consumed during a switching cycle for an adiabatic CMOS circuit is given by:

$$E_{total} = 2I_{off} V_{dd} T \left(1 + \frac{V_t^2}{V_{dd}^2}\right) + \frac{2C_L^2 V_{dd}^2 R_s}{T} \qquad (7)$$

This energy consumption diverges when T→0 and T→∞. It has a minimum for a certain power clock time period, which can be easily calculated from Eq (7). In the case of NEM switches, there is no leakage current owing to an air gap between the terminals during the off-state of the switch [18-24]. However, energy is spent in bending the cantilever to make the switching occur. This bending results in the storage of potential energy in the cantilever. Further, the capacitance of the switch increases as it bends. Therefore, a small amount of energy is required to charge this increased capacitance to the working potential. However, once this energy is spent, the charges are then transferred to the load capacitance through the contact resistance, thus raising the potential of the load capacitance and completing the switching action. This also results in the loss of a small amount of energy. The total energy lost in a NEM switch during switching action can be calculated as:

$$E_{switching} = \frac{1}{2} \times \Delta C_{switch} \times V_{dd}^2 + \frac{1}{2} \times k \times d^2 + \frac{2C_L^2 V_{dd}^2 R_c}{T} \qquad (8)$$

$$E_{switching} = \frac{C_s V_{dd}^2}{4} + \frac{Ewt^3 d^2}{8L^3} + \frac{2C_L^2 V_{dd}^2 R_c}{T} \qquad (9)$$

Where,

$$C_s = \frac{\varepsilon_0 A}{d} \qquad (10)$$

where ε0 is the dielectric constant, A is the area of the NEM switch capacitance, d is the deflection of the switch (distance between the source and gate plates), Rc is the contact 4 of 10 resistance between the switch cantilever and the drain contact, E is Young's modulus of the cantilever and w, t and L are the width, thickness, and length of the cantilever, respectively. This energy is in addition to the energy dissipated in the series resistance of the power supply. Hence, the total energy lost in a switching cycle of an adiabatic NEM switch can be calculated as:

$$E_{total} = \frac{C_s V_{dd}^2}{4} + \frac{Ewt^3 d^2}{8L^3} + \frac{2C_s^2 V_{dd}^2 R_s}{T} + \frac{2C_L^2 V_{dd}^2 R_c}{T} \qquad (11)$$

Now, the mechanical energy stored in the bent cantilever is not completely lost and therefore this energy can be recovered using energy reversible NEM switches.

These switch designs take advantage of the overshoot in the cantilever to reduce the pull-in voltage. In the bent cantilever, Figure 3, when the gate voltage is lowered, the can- tilever is released due to elastic forces and overshoots from its equilibrium position. This overshoot can be utilized by having another gate opposite to the first one. The overshoot reduces the distance between the cantilever and the second gate, thus reducing the pull- in voltage considerably [25]. Once the cantilever is released by the second gate, the same mechanism can be used to operate the switch essentially at a much lower pull-in voltage.

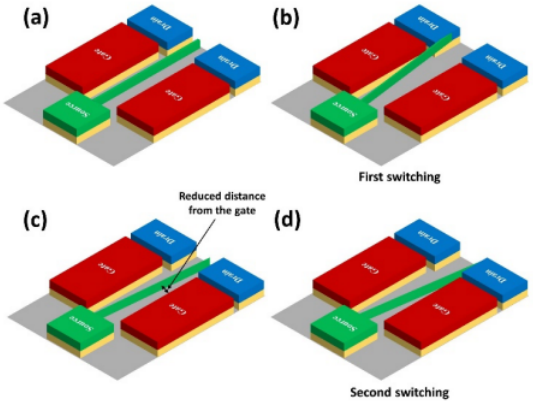

Figure 3: Multi-cycle switching of energy reversible silicon NEM switch has the potential to reduce the pull-in voltage. (a) The as-fabricated switch (b) first switching by application of gate potential (c) the release of the switch causes it to move towards the other gate electrode because of mechanical inertia (d) second switching potential is applied to capture the switch at a position much closer to the gate electrode, hence reducing pull-in voltage for subsequent cycles.

This mechanism makes sure that we have not lose the mechanical energy in the bent cantilever. The energy lost due to air damping can be neglected since the size of the can- tilever, particularly its thickness, is very small [26-29]. Thus, the total power loss during a switching cycle is given by:

$$E_{total} = \frac{C_s V_{dd}^2}{4} + \frac{2C_s^2 V_{dd}^2 R_s}{T} + \frac{2C_L^2 V_{dd}^2 R_c}{T} \quad (12)$$

Also, since the pull-in voltage is much lower, the Vdd can be reduced, which further reduces the energy consumption. Although the NEM switches have been realized in various configurations and materials [30-40], all of them involve a moving beam or a membrane; hence the above analysis can be approximately applied. Also, several studies have demonstrated energy reversibility in NEM switches [41,42]. In this study, we have analyzed the possible use of these devices for adiabatic computing. We have utilized the principle of energy reversibility to experimentally demonstrate the lowering of pull-in voltage of NEM switches.

NEM Switch Array Fabrication and Experimental Analysis

The starting point of experimental verification of energy reversible NEM switches was the development of a process for lateral NEM switches. In this work, we have fabri- cated Silicon-on-Insulator (SoI) based NEM switches in arrays using SoI as a substrate (with 90nm thick SoI and 145nm thick buried oxide). We have doped the partially de- pleted SoI layer with Boron using the ion-implantation. A CMOS compatible process was used to etch the silicon active layer up to the sacrificial oxide (BOX), an amorphous metal (alloyed metal Ti or W nitride) based vertical passivation layers were formed along the sidewall of the silicon switch (cantilever/fin) and a gas phase release was done using va- por Hydro-Fluoric (HF) acid. The device footprint is thus independent of the beam thick- ness and is only a function of the beam width and gap. This architecture is advantageous for scaling and arraying for Large Scale Integration (LSI) Chips. The NEM structures (like a single clamped hanging cantilever) are formed with just one lithography step followed by dry etch and gas-phase release. The final fabricated and released devices are presented in Figure 4.

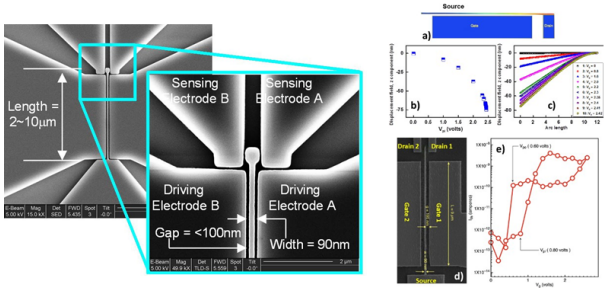

Figure 4: Top View of Electron Micro-graph of the released NEM Switch with 90nm Width and 100nm gap in between Gate and Cantilever.

The fabricated devices were probed using the patterned contact pads for the source, drain, and gate. Here, we have used the Keithley 4200SCS semiconductor parameter ana- lyzer to obtain the electrical performance of the fabricated devices. The operation (I-V) characteristic of a device is presented in Figure 5.

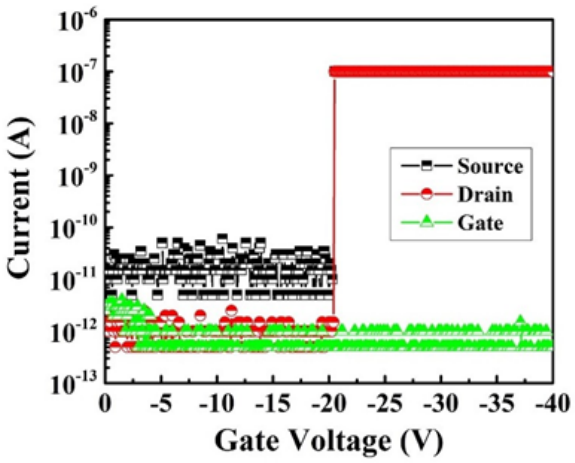

Figure 5: Electrical Characteristics of a NEM Switch with L=2μm and d=100nm with -20.5V observed pull-in voltage.

We have obtained the pull-in voltage, for this device by extrapolating the line of maximum Tran's conductance to the gate voltage axis, as -20.5V. It was found that the source and drain currents follow each other well, particularly after the cantilever has switched. Compliance of 100nA was set for the cantilever current so that the contacts do not get "welded", and there is a pull-out of the switch for multi-cycle operation. Here, a 4th order of magnitude surge in current for a very small change in the applied voltage has been observed. For a device with larger length (L=10 μm), the pull-in voltage for the first switching activity was found to be -5.82V. The Figure 6(a) shows the hysteresis behavior of this device under several cycles of gate voltage. It can be seen that once the device has been switched, the mechanical energy of switching stays within the device, and the pullin voltage reduces to -5.62V, -5.38V, -5.06V (i.e, up to 9%) for the second, third and fourth cycles, respectively (Figure 6(b)). This reduces the energy

needed for subsequent switching of the device, as predicted theoretically.

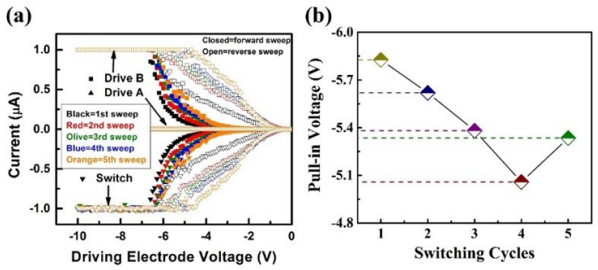

Figure 6: (a) The hysteresis behavior of this device (b) Multi-cycle switching of energy reversible silicon NEM switch shows a reduction in pull-in voltage. The closed symbols represent forward sweep, while the open symbols represent reverse sweep.

The pull-in voltage does not always decrease with consecutive cycles, as reported by other researchers [43,44]. Here, the natural system damping, however small, and friction effects will eventually dampen out any "pendulum system" actuated under conversion of static potential energy to kinetic energy.

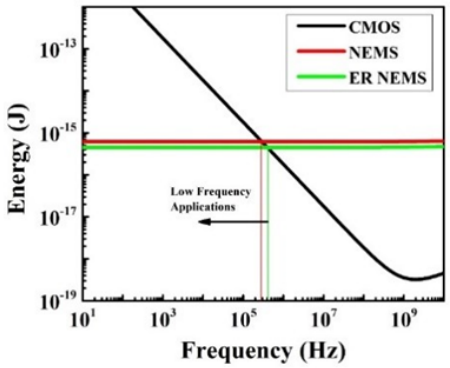

Figure 7: Energy dissipation per cycle of power clock as a function of power clock frequency for Adiabatic CMOS, NEM Switched and Energy Reversible NEM Switches.

The energy needed to switch can be calculated based on the analysis presented pre- viously. The variables in Equations (7), (11), and (12) are assumed to have values accord- ing to Table I. With these values, we obtain the energy dissipation per clock cycle for various frequencies of the applied power clock, Figure 7. This comparison shows that NEM switches, and in particular energy reversible NEMS, tend to dissipate lower energy per clock cycle for low-frequency operations compared to adiabatic CMOS circuits.

This experimental analysis shows that the adiabatic NEM switches can be used for low-frequency biomedical applications where low power consumption is of critical importance [45-47] over high-speed computational performances.

Parameter	Value
Vdd	0.9 Va)
Vpi1	5.82 V
Vpi2	5.05 V
Vt	0.026 V
ε0	8.85 pF/m
A	0.8 μm2
D	100 nm
Cs	70.8 aF
Rs	1343 Ohma)
Cl	141.6 aFb)
E	169 GPa
W	80 nm
T	90 nm
L	10 μm

TABLE I: The state-of-the-art values of different variables used in the theoretical analysis aITRS Tables, 2012. bTwice the value of gate capacitance.

Conclusion

In this work, we presented an energy reversible NEM switch in adiabatic circuitry as a step forward for energy-efficient adiabatic computing device. The pull-in voltage of the device reduces with every switching activity for five cycles and reported a pull-in voltage of 5V. Logic circuits based on such low-power NEM switches, in adiabatic configuration, can complement conventional CMOS circuits for low frequency applications. It is shown that the theoretical analysis and experimental benefits of using NEM switches (three terminals and energy reversible, both) in adiabatic circuits, in terms of the energy dissipation per unit cycle of power clock for various power clock frequencies is better in place of conventional Complementary Metal Oxide Semiconductor (CMOS) transistor switches. The experimental results illustrate that the reduction in pull-in voltage (13%) for subsequent cycles of switching for energy reversible NEM switches, indicate a reduction in switching energy. Therefore, it may be established that the NEM switches promise to offer lower energy consumption for low frequency operations (<100 kHz) and therefore is best suited for biomedical applications.

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